Amended Claims

1. An ATM cell processor comprising a line interface, a backplane interface, and a processing means between the interfaces for processing cells according to their headers, characterised in that:-

the processing means comprises a segmentation and reassembly (SAR) interface (25);

the processing means comprises a queueing function (12) comprising means for controlling transfer of cells to the line interface (15) and to the SAR interface (25) according to the cell headers; and

the processing means further comprises a mapping function (16) comprising means for changing cell headers during transfer from the line interface (15) to the backplane interface (11) according to mapped cell destinations.

2. An ATM cell processor as claimed in claim 1, wherein the queueing function (12) comprises means for receiving control cells from the SAR interface (25).

3. An ATM cell processor as claimed in ~~claims 1 or 2,~~ claim 1 wherein the processing means further comprises a cell memory controller (13) for interfacing with an external cell memory, and the queueing function (12) comprises means for accessing a cell memory via said controller (13).

4. An ATM cell processor as claimed in ~~any preceding claim,~~ claim 1 wherein the processing means further comprises a control memory controller (14) for interfacing with an external control memory, and the queueing function (12) comprises means for accessing a control memory via said controller (14).

5. An ATM cell processor as claimed in ~~claims 3 or 4~~ claim 3, wherein the queueing function (12) comprises means for dequeueing from a cell memory and for tracking the cells using pointer information retrieved from a control memory.

6. An ATM cell processor as claimed in ~~claims 4 or 5~~ claim 4, wherein the processing means further comprises a configuration and status function (21) connected to the queueing function (12) and to the control memory controller (14), and means (20) for allowing an external microprocessor access said control memory for initial setup and configuration and subsequent status monitoring.

7. An ATM cell processor as claimed in ~~any preceding claim~~ claim 1, wherein the queueing function (12) comprises means for managing path descriptor tables (30) in a control memory.

8. An ATM cell processor as claimed in claim 7, wherein the queueing function comprises means for using the VPI of an incoming cell to form an offset into the path descriptor table.

9. An ATM cell processor as claimed in ~~any preceding claim~~ claim 1, wherein the queueing function (12) comprises means for managing queue description tables, each relating to individual queues, in the control memory.

10. An ATM cell processor as claimed in ~~any preceding claim~~ claim 1, wherein the queueing function (12) comprises means for managing a queue server matrix, the location and size of which is indicated by configuration registers, and in which each element of the matrix stores a plurality of fields and each field is associated with a queue.

11. An ATM cell processor as claimed in claim 10, wherein the queueing function (12) comprises means for checking queues in ascending order in an element by starting with a most significant byte in the fields of each element.

12. An ATM cell processor as claimed in claim 1 ~~any preceding claim~~, wherein the queueing function (12) comprises means for maintaining a plurality of queue storage pool heaps by maintaining a set of pointers programmed using configuration registers.

13. An ATM cell processor as claimed in claim 1 ~~any preceding claim~~, wherein the mapping function (16) comprises means for adding an additional header to a cell for internal control signalling.

14. An ATM cell processor as claimed in claim 13, wherein the mapping function (16) comprises means for passing cells to the queueing function (12), for passing cells to the backplane interface (11), and for dropping cells.

15. An ATM cell processor as claimed in claim 14, wherein the mapping function (16) comprises means for maintaining tables in a control memory.

16. An ATM cell processor as claimed in claim 15, wherein the tables comprise a per port statistics table storing data indicating the numbers of cells with invalid and disabled VPI/VCIs and with unsupported PTIs.

17. An ATM cell processor as claimed in claim 15 ~~or 16~~, wherein the tables comprise a VCC connection table containing the following information on a per connection basis:-

mapping descriptor,

received cell count,

dropped cell count, and

GCRA words.

18. An ATM cell processor as claimed in CLAIM 1 ~~any preceding claim~~, wherein the processing means further comprises a policing function (17) comprising means for monitoring traffic characteristics.

19. An ATM cell processor as claimed in claim 18, wherein the policing function (17) is connected between the mapping function (16) and the backplane (11) and comprises means for monitoring traffic characteristics of cell streams outputted by the mapping function (16) to the backplane interface (11).